Deborah A. Wallach

kerr@lcs.mit.edu
545 Technology Square, Rm 520
Cambridge, MA 02139
(617) 253-7436

37 Bristol Street
Cambridge, MA 02141
(617) 876-6327

Education

Massachusetts Institute of Technology
Ph.D. in Computer Science with a minor in VLSI. Expected, December 1996.
Thesis title: Supporting application-specific libraries for communication.
Thesis Committee: M. Frans Kaashoek, David D. Clark, William E. Weihl.

S.M. in Computer Science (1992).
Thesis title: PHD: A hierarchical cache coherence protocol. Supervisor: William J. Dally.

S.B. in Computer Science (1990) with a concentration in Psychology.

Undergraduate and graduate G.P.A.: 5.0/5.0.

Professional Experience

MIT Laboratory for Computer Science—Research Assistant **Sep. 1993–present**
I worked on the problem of providing a general communication interface with the high performance of more restricted models in a distributed system environment (see attached thesis abstract) [3,1,7]. To support my thesis, I developed infrastructure for my own and group research activities by putting together a four-processor DECstation 5000 system to which I: ported and improved a DEC AN2 ATM network device driver for Aegis (an exokernel operating system), designed and implemented an OS interface for the AN2, helped implement several networking software layers including the TCP/IP protocol stack, and wrote client-server applications which use the networking software layers.

Thinking Machines Corporation—Consultant **June 1993–June 1994**
I consulted for the Connection Machine Scientific Software Library (CMSSL) group, which provides heavily optimized libraries to users of the Connection Machine 5 (CM-5). I worked independently on two projects: parallel sort and parallel histogram, designing and implementing code to speed up the currently existing versions of these applications.

MIT Artificial Intelligence Laboratory—Research Assistant **Sep. 1989–May 1993**
The MIT J-Machine multicomputer was constructed to study the role of a set of primitive mechanisms in providing efficient support for parallel computing. Each J-Machine node consists of an integrated multicomputer component, the Message-Driven Processor (MDP), and 1 MByte of DRAM. The MDP provides mechanisms to support efficient communication, synchronization, and naming. A 1024-node J-Machine is currently operational. As a researcher involved in this project, I contributed to the design and implementation of the MDP chip, as well as to the software infrastructure for the machine. Along with two others, I evaluated the mechanisms that the machine provides, measuring them directly as well as in the context of four complete applications [4].

MIT Artificial Intelligence Laboratory—Research Assistant **Sep. 1989–Sep. 1992**
I designed a protocol for coherent caching using hierarchical directories. This protocol can be used to emulate a shared-memory environment for massively parallel message-passing architectures such as the J-Machine. The protocol is intended to allow a programmer to use a shared-memory abstraction without worrying about data location, while preserving locality and scalability. I also introduced a method of describing locality for hierarchical protocols and employed this method in the derivation of two models used to study the protocol behavior.

Thinking Machines Corporation—Software Engineer **June 1990–August 1990**
As part of the Twuffle Project, whose goal was to reduce the time needed to perform regular patterns of communication using the hypercube network of the Connection Machine 2 (CM-2), I designed, implemented, and tested low-level tools to shuffle, transpose, and (un)gray-code local blocks of data.

MIT Artificial Intelligence Laboratory—UROP **January 1989–June 1989**
Designed at both a register-transfer level and a schematic level an internal memory interface for the Concurrent VLSI Architectures Group's Message-Driven Processor (MDP) chip. Verified both designs with a simulator.

AT&T Bell Laboratories—Technical Assistant **Summers 1986–1989**

1989 Designed and wrote a simulator of a VME board to coordinate the parallel operation of 16 SMOKE (32 bit floating-point processor) chips sharing four memory elements. The resulting system was designed to be plugged directly into a Sun-3 host to test the SMOKE chips.

1988 Added line detection capabilities and automatic thresholding to the Boie-Cox edge detector. The edge detector previously erroneously marked lines as two closely spaced edges [6]. Participated in testing of and data processing for the Cox-Kruskal subpixel registration algorithm [5].

1987 Wrote an absolute debugger for the 3b5 under System V Release 3 UNIX in C with multiprocess capability. Learned about parsers and device drivers.

1986 Designed and wrote a database manager for the POST electronic mail system in C.

NASA Ames Research Center—Laboratory Assistant **June 1985–June 1986**
Participated in the Summer High School Apprentice Research Program. Helped write, test, and run a C program which calculated human visual contrast thresholds. Wrote a program to compress image data based on using less information to store the portion of the image not currently in focus.

Academic Honors and Prizes

Intel Corporation
Intel Foundation Graduate Fellowship recipient (1995–1996).

Office of Naval Research
American Society of Engineering Education Fellowship recipient (1990–1994).

Massachusetts Institute of Technology
Received the 1989 G. C. Newton Undergraduate Prize for the best undergraduate EECS laboratory project.
Received letters of commendation in Laboratory in Software Engineering and Introductory Digital Systems Laboratory.

AT&T Bell Laboratories
AT&T Engineering Scholarship Program Participant (full undergraduate four year scholarship).
Recipient of the 1989 AT&T Distinguished Scholars Award.

Honorary Societies and Service

Program committee member, 5th Annual MIT Student Workshop on Scalable Computing, 1995.
Member of student committee to recommend revision to the MIT Computer Science Graduate curriculum, 1995.
Member of the Tau Beta Pi and Eta Kappa Nu Honor societies. Inducted into both February 1989.
Associate member of Sigma Xi, inducted 1992.

References

Professor M. Frans Kaashoek; MIT Laboratory for Computer Science; 545 Technology Square; Cambridge, MA 02139. (617) 253-7149. Email: kaashoek@lcs.mit.edu.

Dr. David D. Clark; MIT Laboratory for Computer Science; 545 Technology Square; Cambridge, MA 02139. (617) 253-6003. Email: ddc@lcs.mit.edu.

Professor William J. Dally; MIT Artificial Intelligence Laboratory; 545 Technology Square; Cambridge, MA 02139. (617) 253-6043. Email: billd@ai.mit.edu.

Professor Lennart S. Johnsson, 592 Philip G. Hoffman Hall, Department of Computer Science, The University of Houston, 4800 Calhoun Road, Houston, TX 77204-3475. (713) 743-3371. Email: johnsson@cs.uh.edu.

Refereed Publications

1. Deborah A. Wallach, Dawson R. Engler, and M. Frans Kaashoek. ASHs: Application-specific handlers for high-performance messaging. In *Proceedings of ACM SIGCOMM'96 Conference on Applications, Technologies, Architectures and Protocols for Computer Communication*, pages 40–52, Stanford, California, August 1996.
2. Kirk L. Johnson, M. Frans Kaashoek, and Deborah A. Wallach. CRL: High-performance all-software distributed shared memory. In *Proceedings of the 15th Symposium on Operating Systems Principles*, pages 213–228, Copper Mountain Resort, Colorado, December 1995.
3. Deborah A. Wallach, Wilson C. Hsieh, Kirk L. Johnson, M. Frans Kaashoek, and William E. Weihl. Optimistic active messages: A mechanism for scheduling communication with computation. In *Proceedings of the 5th Symposium on Principles and Practice of Parallel Programming*, pages 217–226, Santa Barbara, California, July 1995.
4. Michael D. Noakes, Deborah A. Wallach, and William J. Dally. The J-Machine multicomputer: An architectural evaluation. In *Proceedings of the 20th International Symposium on Computer Architecture*, pages 224–235, San Diego, California, May 1993. IEEE.
5. Ingemar J. Cox, Joseph B. Kruskal, and Deborah A. Wallach. Predicting and estimating the accuracy of a subpixel registration algorithm. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, 12(8):721–734, August 1990.
6. Ingemar J. Cox, Robert A. Boie, and Deborah A. Wallach. Line recognition. In *Proceedings of the Tenth International Conference on Pattern Recognition*, pages 639–645. IEEE, June 1990.

Workshops

7. M. Frans Kaashoek, Dawson R. Engler, Gregory R. Ganger, and Deborah A. Wallach. Server operating systems. To appear in *Seventh SIGOPS European Workshop: Systems Support for Worldwide Applications*, September 1996.
8. M. Frans Kaashoek, William E. Weihl, Deborah A. Wallach, Wilson C. Hsieh, and Kirk L. Johnson. Optimistic active messages: Structuring systems for high-performance communication. In *Sixth SIGOPS European Workshop: Matching Operating Systems to Application Needs*, Sep. 1994.

Extracurricular Activities and Accomplishments

Secretary of the Student Information Processing Board (SIPB) for one year, member of the Executive Committee for two years. Volunteer Online Consultant for Project Athena for three years. Hobbies include: ice hockey, horseback riding, running, and rollerblading.